

**ABSTRACT**

Please replace the existing Abstract with the following new Abstract:

A clock multiplier circuit which generates a multiple clock having a stable frequency from a reference clock without using analog devices. The clock multiplier circuit includes a ring oscillator which oscillates at a higher frequency than that of the multiple clock; a reference clock counter for counting the sampling output of the reference clock by the output clock of the ring oscillator to obtain a count value of the half cycle of the reference clock; and a multiple clock counter which, in case the value obtained by dividing the count value of the half cycle of the obtained reference clock by the multiplication factor externally given is defined as a multiple count value, inverts the multiple clock output each time it counts the multiple count value by the output clock of the ring oscillator.